IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No.: **AZMT/002P1**	§	Serial No.: **10/730,758**
	§	
Filed: **December 8, 2003**	§	Group Art Unit: **2814**
	§	
In re Application of: **Nallan, et al.**	§	Confirmation No.: **3464**
	§	
	§	Examiner: **Ha, Nathan W.**

For: **METHOD AND APPARATUS FOR PACKAGING ELECTRONIC COMPONENTS**

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CORRECTED APPEAL BRIEF

In response to the Notification of Non-Compliant Appeal Brief dated September 15, 2006, please enter this Corrected Appeal Brief. This Brief is identical to the Appeal Brief originally filed June 20, 2006 with the exception of the correction to delete withdrawn claims 12-14 from the listing of the claims in the Claims Appendix.

As this response is submitted within one month from the date of mailing of the Notification of Non-Compliant Appeal Brief, the Appellant believes that no fees are due in connection with this response. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees, required to make this response timely and acceptable to the Office.

REAL PARTY IN INTEREST

The real party in interest is Azimuth Industrial Co., Inc., located in Union City, California.

RELATED APPEALS AND INTERFERENCES

The Appellant knows of no related appeal and/or interference that may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-14 are pending in the application. Claims 12-14 are withdrawn from consideration. Claims 1-11 stand rejected in view of several references as discussed below. The rejection of claims 1-11 based on the cited references is appealed. The pending claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

No amendments to the claims were submitted in this application subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a method of packaging at least one component. In the embodiment of independent claim 1, a method of packaging at least one component includes providing a lid 104 having a plurality of vent holes 105. (¶ [0021]; Figs. 3, 7.) Sidewalls 302 are molded onto a substrate 202 to form a plurality of cavities 300 surrounding a component-mounting surface (ground plane 208). (¶[0020]; Figs. 2-3, 7.) A component 306 is mounted on the component-mounting surface 208 in each cavity 300. (¶ [0024]; Figs. 3, 7.) A curable adhesive 500 is applied to a top surface 310 of the sidewalls 302. (¶ [0025]; Figs. 5-7.) The lid 104 is placed upon the top surface 310 of the sidewalls 302 such that at least one vent hole 105 is aligned with each cavity 300. (¶ [0026]; Figs. 3, 7.) The adhesive 500 is then cured, wherein said vent hole 105 provides a path for outgassing during curing. (*Id.*) Said vent holes 104

are then sealed to form a component package assembly having a plurality of cavities 300, separated by sidewalls 302. (¶ [0027]; Figs. 5-7.) The component package assembly 116 is separated into a plurality of individual component packages 118. (¶ [0028]; Figs. 6-7.)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-7 and 9-11 stand rejected under 35 USC §103(a) as being obvious in light of United States Patent No. 6,268,236, issued July 31, 2001 to *Miyawaki* (hereinafter *Miyawaki*) in view of United States Patent No. 4,897,508 issued January 30, 1990 to *Mahulikar, et al.*, (hereinafter *Mahulikar*).

2. Claim 8 stands rejected under 35 USC §103(a) as being obvious in light of *Miyawaki* in view of *Mahulikar*, as applied above, and further in view of United States Patent No. 5,776,799, issued July 7, 1998 to *Song, et al* (hereinafter *Song*).

ARGUMENT

1. Claims 1-7 and 9-11

As noted above, claims 1-7 and 9-11 stand rejected as being unpatentable over *Miyawaki* in view of *Mahulikar*. The Appellant disagrees.

To reject a claim under 35 USC §103, the initial burden is on the Examiner to create a *prima facie* case of obviousness. One of the basic criteria to meet this burden is that the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP* §2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Here, the cited references fail to teach or suggest the specific steps recited in independent claim 1. Specifically, the cited references fail to teach or suggest molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface in combination with the other limitations recited in claim 1.

The Examiner contends that *Miyawaki* "discloses a method of packaging at least one component, comprising: providing a lid 2; molding sidewalls 1B, for example, onto a substrate to form a plurality of cavities 4 surrounding a component-mounting surface; mounting a component 7 on the component-mounting surface in each capacity,

applying a curable adhesive 3 to a top surface of the sidewalls; placing the lid upon the surface of the sidewall; curing said adhesive; and separating the component package into a plurality of individual component packages." (*Final Office Action*, ¶2; citing *Miyawaki*, Figs. 2A-2C). The Appellant respectfully disagrees.

With reference to Figures 2A-2C, and in all other embodiments, *Miyawaki* clearly teaches that the base package substrate 1 is created by bonding together a lower first substrate 1A and an upper second substrate 1B having a grid-like pattern of rectangular through-holes. (*Miyawaki*, col. 2, l. 66 – col. 3, l. 1; Figs. 2A-2C.) Both the lower first substrate 1A and upper second substrate 1B (containing the pattern of through-holes that form the sidewalls of the package) are formed prior to being adhered to one another. For example, at col. 3, ll. 8-12, the reference teaches, "(t)hrough holes or penetrating holes are formed in the second (upper) substrate 1B in order to produce hollow cavities." The substrates 1A and 1B are then "stacked into the single base substrate 1, thereby constituting a substrate having a plurality of cavities." Clearly, the method of bonding the upper second substrate 1B to the lower first substrate 1A, as taught by *Miyawaki*, does <u>not</u> teach nor suggest molding sidewalls onto a substrate to form a plurality of cavities, as recited in Appellant's claim 1.

In the Response to Arguments section of the Final Office Action dated October 13, 2005, the Examiner responded to the Appellant's argument by stating that the molding feature mentioned by *Miyawaki* is a "well known conventional process;" that because the teachings of *Miyawaki* claim to attain the same sealing and separation characteristics of molding and productivity of a molding process it renders obvious the process of creating cavities by a molding process; and that molding is a conventional process in semiconductor packaging. The Examiner concludes that because of these statements, the references "in fact discloses all of the claimed limitations." (Final Office Action, p. 4, l. 20 – p. 5, l. 10.)

Furthermore, in the Advisory Action dated January 18, 2006, the Examiner again responds to Appellant's arguments by asserting that "several methods of forming a substrate are discussed [in *Miyawaki*]. For instance, *Miyawaki* discusses that the hollow package, or cavity, can be formed by using conventional molding method, and this method is well known and commonly used." The Examiner asserts that this disclosure

teaches or suggests the step of molding sidewalls onto a substrate. (*Advisory Action*, p. 3). The Appellant disagrees.

With respect to the "conventionality" of molding processes, even if molding is a conventional process in the semiconductor packaging industry, the Examiner has not pointed to a single reference or combination of references, or presented convincing line of reasoning that teaches all the limitations recited in the method of packaging at least one component as presently claimed by Appellant. To meet the burden of creating a *prima facie* case of obviousness, the Examiner must show that the combination of references teaches all of the limitations recited in the claims.

Even assuming, *arguendo*, that all of the Examiner's statements above with respect to the "molding process" are true, the Examiner has not pointed to a single portion of *Miyawaki* or to any other reference that teaches or suggests the limitations as presently recited in claim 1. The only reference to molding in *Miyawaki* is the reference to a commonly-used "mold package" or "transfer mold package" mentioned in the background of the invention. (*Miyawaki*, col. 1, ll. 15-58.) *Miyawaki* is completely devoid of any teaching or suggestion relating to any of the steps that are performed to create this "commonly-used" mold package. In fact, the purpose of the teachings of *Miyawaki* is to provide a method of packaging a semiconductor device that overcomes the deficiencies of the conventional mold packaging cited by the Examiner. (*Id.*)

For example, *Miyawaki* clearly differentiates between the use of a hollow cavity and a molded cavity for encapsulating a component. (*See, at least, Miyawaki*, col. 1, ll. 16-25). In the Background of the *Miyawaki* patent, *Miyawaki* states that although a "commonly-used mold package" may be used to encapsulate components, there are drawbacks associated with this method. (*Id.*) *Miyawaki* describes one such molding method where "a substance, such as epoxy resin having a large dielectric constant comes into close contact with a semiconductor chip…thereby introducing parasitic capacitance and deteriorating the characteristics of the semiconductor package." (*Id.*) Throughout the disclosure, *Miyawaki* emphasizes that his embodiments overcome the drawbacks associated with this type of molding process while achieving similar benefits as those attained through this type of molding process. (*See, at least, Miyawaki*, col. 4, ll. 51-60, and col. 8, ll. 4-7). However, as noted above, at no place in *Miyawaki*, either

at the location cited by the Examiner or elsewhere, is any specific molding process taught or suggested, let alone one that includes the step of molding sidewalls onto a substrate to form a plurality of cavities, as recited in claim 1.

Thus, rather than "render[ing] [obvious] the process of creating cavities by [a] molding process," (as asserted by the Examiner in the *Final Office Action*, p. 5, ¶4), in fact, *Miyawaki* actually teaches away from using conventional mold packages due to the drawbacks associated with those mold packages (*e.g.*, parasitic capacitance and deterioration of the high-frequency characteristics of the semiconductor device). Therefore, *Miyawaki* fails to teach or suggest molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1.

In the Advisory Action dated January 18, 2006, the Examiner further asserts that "[f]or example, fig. 2C shows a few substrates that have sidewalls molded onto, so a better sealing may be established." (*Advisory Action*, p. 3)(emphasis added). However, contrary to the Examiner's assertion, and as noted above, the entire detailed description of *Miyawaki*, including the description of Figure 2C, is entirely devoid of any mention of any type of molding process. In fact, rather than showing substrates that have sidewalls molded onto, Figure 2C of *Miyawaki*, actually shows multiple cavities created by bonding a lower first substrate 1A and a pre-formed upper second substrate 1B to create a base substrate 1, followed by the sealing of a cap member 2 by adhesive 3. (*Miyawaki*, col. 2, l. 66 – col. 3, l. 1; col. 3, ll. 19-24.)

As discussed above, *Miyawaki* discloses a method of forming an semiconductor device package that overcomes the problems associated by conventional molding processes. Thus, the embodiments cited by the Examiner (and all other embodiments taught or suggested by *Miyawaki*) fail to disclose a "substrate having sidewalls molded onto," but rather show the bonded upper and lower preformed substrates as taught by *Miyawaki* to overcome the drawbacks of the molding process. As such, *Miyawaki* fails to teach or suggest molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1.

As further evidence of the lack of suggestion or motivation to modify the teachings of *Miyawaki*, the Appellant points out that if the method of forming the packages of *Miyawaki* were modified by the "conventional" mold package disclosed by

Miyawaki, the modification would render *Miyawaki* unsatisfactory for its intended purpose. As noted above, the purposed of the teachings of *Miyawaki* is to provide a method of packaging a semiconductor device that overcomes the deficiencies of the conventional mold packaging cited by the Examiner. Modifying the teachings of *Miyawaki* to include the conventional prior art method that *Miyawaki* is trying to avoid would render Miyawaki unsatisfactory for its intended purpose. The Federal Circuit has held that "if [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); *see also, MPEP* §2143.01.

Therefore, per *In re Gordon* and *MPEP* §2143.01, there is no suggestion or motivation to make the proposed modification because the proposed modification of the method of *Miyawaki* would render the method of *Miyawai* unsatisfactory for its intended purpose. Accordingly, a *prima facie* case of obviousness has not been established because there is no suggestion or motivation to make the proposed modification.

The Examiner cites *Mahulikar* as teaching an analogous package including a substrate, a cavity, and a component in the cavity, with an adhesive layer to attach a lid to the substrate, with the lid comprising a vent hole for releasing reaction by-products generated during the cure cycle. The Examiner concludes that a combination of the teachings of *Miyawaki* and *Mahulikar* teaches the Appellant's invention as recited in the rejected claims. (*Final Office Action*, ¶2). The Appellant respectfully disagrees.

With respect to *Mahulikar*, by inspection of any of FIGS. 1, 3, or 4 (and the corresponding written descriptions), it is easily determined that *Mahulikar* teaches fastening a leadframe 16 to a base 12 with a first sealant 28 and subsequently fastening a cover component 14 to the leadframe 16 with a second sealant 26 (*see, at least, Mahulikar*, col. 3, ll. 21-24; col. 4, ll. 8-12). Thus, as applicable here, *Mahulikar* teaches nothing more than sealants applied for bonding the base, leadframe, and cover component. Therefore, *Mahulikar* fails to teach or suggest a modification to the teachings of *Miyawaki* that would result in a method including the step of molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1.

Accordingly, a *prima facie* case of obviousness has not been established because the combination of *Miyawaki* and *Mahulikar* fails to yield a method of packaging at least one component including the step of molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1, and all claims depending therefrom.

Thus, independent claim 1 and claims 2-7 and 9-11, depending therefrom, are patentable over *Miyawaki* in view of *Mahulikar*. Accordingly, the Appellant requests that the rejection be withdrawn and the claims allowed.

2. Claim 8

As noted above, claim 8 stands rejected as being unpatentable over *Miyawaki* in view of *Mahulikar*, as applied above, and further in view of *Song*. The Appellant respectfully disagrees.

Independent claim 1, from which claim 8 depends, recites limitations not taught or suggested by any permissible combination of the cited art. The patentability of claim 1 over the combination of *Miyawaki* in view of *Mahulikar* is discussed above. The Examiner cites *Song* to show forming an adhesive layer by screen printing. However, *Song* fails to teach or suggest a modification to the combination of *Miyawaki* in view of *Mahulikar* in a manner that would result in a method of packaging at least one component including the step of molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1. As such, a *prima facie* case of obviousness has not been established because the cited combination fails to yield the limitations recited in claim 1.

Thus, claim 8 is patentable over *Miyawaki* in view of *Mahulikar* and further in view of *Song*. Accordingly the Appellants respectfully request that the rejection be withdrawn and the claim allowed.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1-11 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Original) A method of packaging at least one component, comprising:

providing a lid having a plurality of vent holes;

molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface;

mounting a component on the component-mounting surface in each cavity;

applying a curable adhesive to a top surface of the sidewalls;

placing the lid upon the top surface of the sidewalls such that at least one vent hole is aligned with each cavity;

curing said adhesive, said vent hole providing a path for outgassing during curing;

sealing said vent holes to form a component package assembly having a plurality of cavities, separated by sidewalls; and

separating the component package assembly into a plurality of individual component packages.

2. (Original) The method of claim 1, wherein the component comprises electronic circuits.

3. (Original) The method of claim 1 wherein the component is a radio frequency circuit.

4. (Original) The method of claim 1, wherein the top cover and sidewalls are formed of polymers.

5. (Original) The method of claim 1, wherein curing said adhesive comprises heating the adhesive.

6. (Original) The method of claim 1, wherein separating comprises sawing, laser cutting, water cutting, milling, machining, lathing, and combinations thereof.

7. (Original) The method of claim 1 wherein placing the lid upon the sidewalls comprises applying a substantially uniform pressure over each cavity.

8. (Original) The method of claim 1 wherein the applying step comprises screen printing the adhesive on the top surface of the sidewalls.

9. (Original) The method of claim 1 wherein the cavity comprises a low dielectric constant material.

10. (Original) The method of claim 9 wherein the low dielectric constant material is air.

11. (Original) The method of claim 9 wherein the component is a radio frequency circuit.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]